

# NVMFD5873NL

## Power MOSFET

60 V, 13 mΩ, 58 A, Dual N-Channel Logic Level, Dual SO-8FL

### Features

- Small Footprint (5x6 mm) for Compact Designs
- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- NVMFD5873NLWF – Wettable Flanks Option for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- This is a Pb-Free Device

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			$V_{DSS}$	60	V
Gate-to-Source Voltage			$V_{GS}$	$\pm 20$	V
Continuous Drain Current $R_{\Psi J-mb}$ (Notes 1, 2, 3, 4)	Steady State	$T_{mb} = 25^{\circ}\text{C}$	$I_D$	58	A
		$T_{mb} = 100^{\circ}\text{C}$		41	
Power Dissipation $R_{\Psi J-mb}$ (Notes 1, 2, 3)		$T_{mb} = 25^{\circ}\text{C}$	$P_D$	107	W
		$T_{mb} = 100^{\circ}\text{C}$		54	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 3 & 4)	Steady State	$T_A = 25^{\circ}\text{C}$	$I_D$	10	A
		$T_A = 100^{\circ}\text{C}$		7.0	
Power Dissipation $R_{\theta JA}$ (Notes 1 & 3)		$T_A = 25^{\circ}\text{C}$	$P_D$	3.1	W
		$T_A = 100^{\circ}\text{C}$		1.6	
Pulsed Drain Current	$T_A = 25^{\circ}\text{C}$ , $t_p = 10\text{ }\mu\text{s}$		$I_{DM}$	190	A
Operating Junction and Storage Temperature			$T_J$ , $T_{stg}$	-55 to 175	$^{\circ}\text{C}$
Source Current (Body Diode)			$I_S$	58	A
Single Pulse Drain-to-Source Avalanche Energy ( $T_J = 25^{\circ}\text{C}$ , $V_{GS} = 10\text{ V}$ , $I_{L(pk)} = 28.3\text{ A}$ , $L = 0.1\text{ mH}$ , $R_G = 25\text{ }\Omega$ )			$E_{AS}$	40	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			$T_L$	260	$^{\circ}\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Junction-to-Mounting Board (top) – Steady State (Notes 2, 3)	$R_{\Psi J-mb}$	1.4	$^\circ\text{C/W}$
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	48	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Psi ( $\Psi$ ) is used as required per JESD51-12 for packages in which substantially less than 100% of the heat flows to single case surface.
3. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
4. Maximum current for pulses as long as 1 second are higher but are dependent on pulse duration and duty cycle.

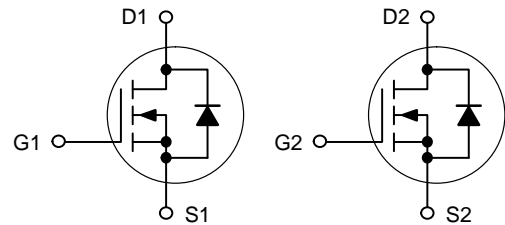


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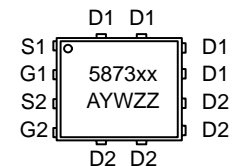
$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	$I_D$ MAX
60 V	13 mΩ @ 10 V	58 A
	16.5 mΩ @ 4.5 V	

### Dual N-Channel



### MARKING DIAGRAM

DFN8 5x6  
(SO8FL)  
CASE 506BT



5873NL = Specific Device Code for NVMFD5873NL

5873LW = Specific Device Code for NVMFD5873NLWF

A = Assembly Location

Y = Year

W = Work Week

ZZ = Lot Traceability

### ORDERING INFORMATION

Device	Package	Shipping†
NVMFD5873NLT1G	DFN8 (Pb-Free)	1500 / Tape & Reel
NVMFD5873NLWFT1G	DFN8 (Pb-Free)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NVMFD5873NL

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>			54.9		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 60 V	T <sub>J</sub> = 25°C		1.0	μA
			T <sub>J</sub> = 125°C		100	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V			±100	nA

### ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	1.5		2.5	V
Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>			-5.8		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 15 A		10.7	13	mΩ
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 10 A		13.6	16.5	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 5.0 V, I <sub>D</sub> = 15 A		15		S

### CHARGES AND CAPACITANCES

Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, f = 1.0 MHz, V <sub>DS</sub> = 25 V		1560		pF
Output Capacitance	C <sub>oss</sub>			145		
Reverse Transfer Capacitance	C <sub>rss</sub>			98		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 48 V, I <sub>D</sub> = 15 A		16.5		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>			1.3		
Gate-to-Source Charge	Q <sub>GS</sub>			4.0		
Gate-to-Drain Charge	Q <sub>GD</sub>			8.8		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 48V, I <sub>D</sub> = 15 A		30.5		nC

### SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 48 V, I <sub>D</sub> = 15 A, R <sub>G</sub> = 2.5 Ω		10.8		ns
Rise Time	t <sub>r</sub>			51		
Turn-Off Delay Time	t <sub>d(off)</sub>			21		
Fall Time	t <sub>f</sub>			42.6		
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 48 V, I <sub>D</sub> = 15 A, R <sub>G</sub> = 2.5 Ω		9.5		ns
Rise Time	t <sub>r</sub>			13		
Turn-Off Delay Time	t <sub>d(off)</sub>			25		
Fall Time	t <sub>f</sub>			6.6		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 15 A	T <sub>J</sub> = 25°C		0.8	1.0	V
			T <sub>J</sub> = 125°C		0.7		
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, dI <sub>S</sub> /dI = 100 A/μs, I <sub>S</sub> = 15 A		22.4			ns
Charge Time	t <sub>a</sub>			14.5			
Discharge Time	t <sub>b</sub>			9.0			
Reverse Recovery Charge	Q <sub>RR</sub>			18			nC

5. Pulse Test: pulse width = 300 μs, duty cycle ≤ 2%.

6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

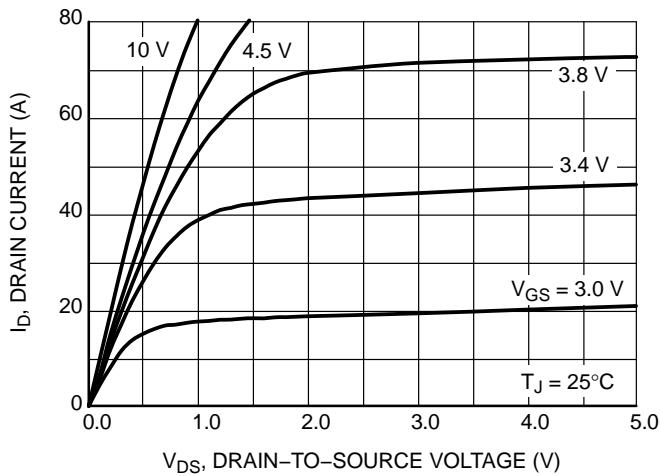


Figure 1. On-Region Characteristics

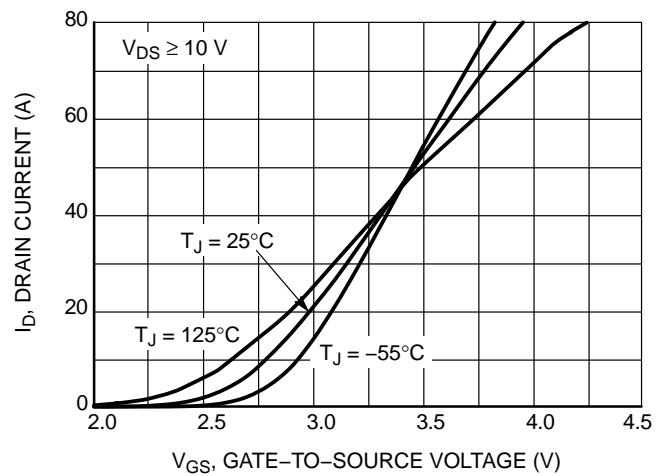


Figure 2. Transfer Characteristics

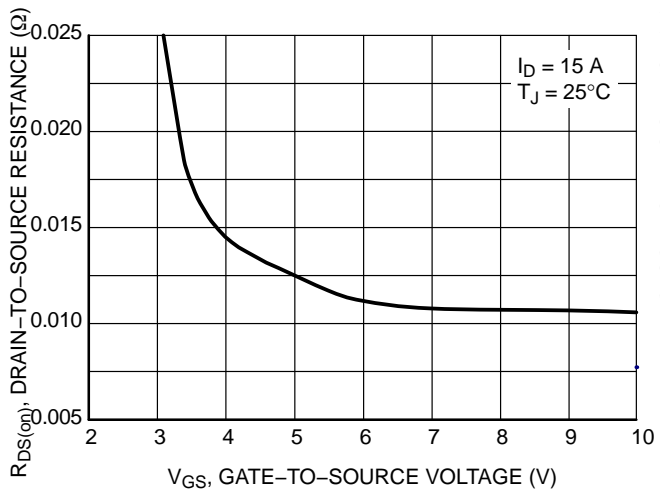


Figure 3. On-Resistance vs.  $V_{GS}$

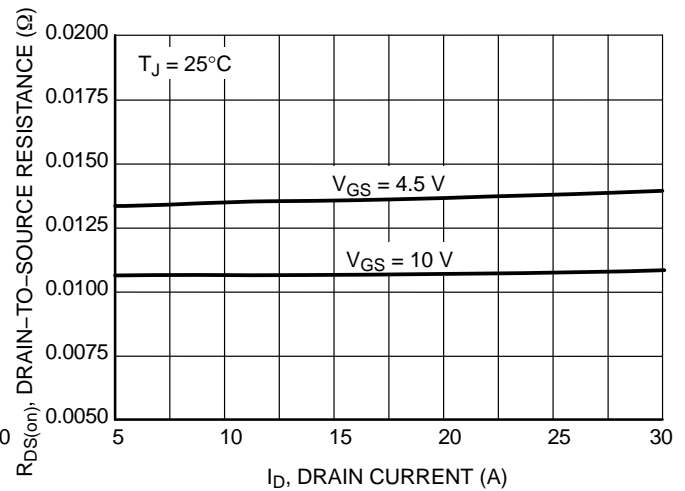


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

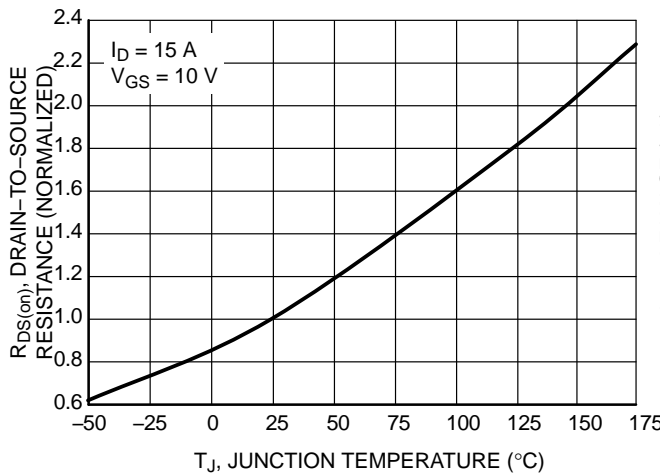


Figure 5. On-Resistance Variation with Temperature

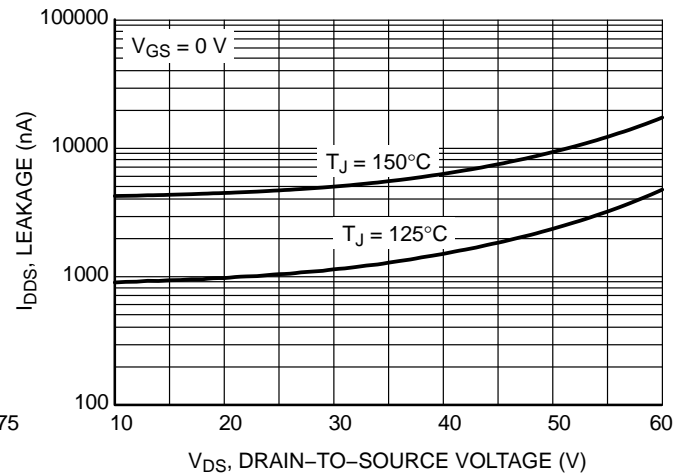


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

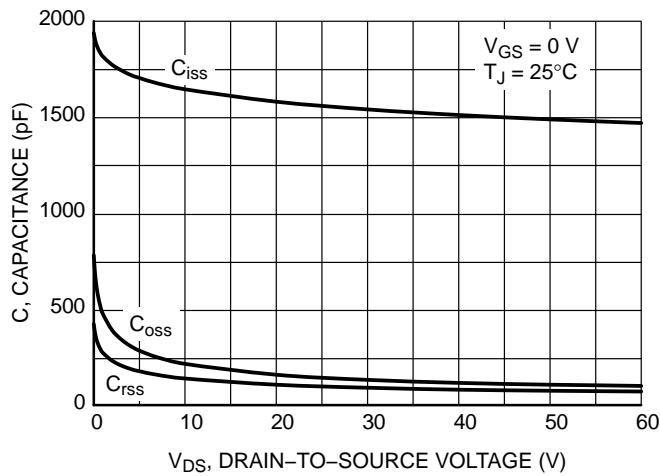


Figure 7. Capacitance Variation

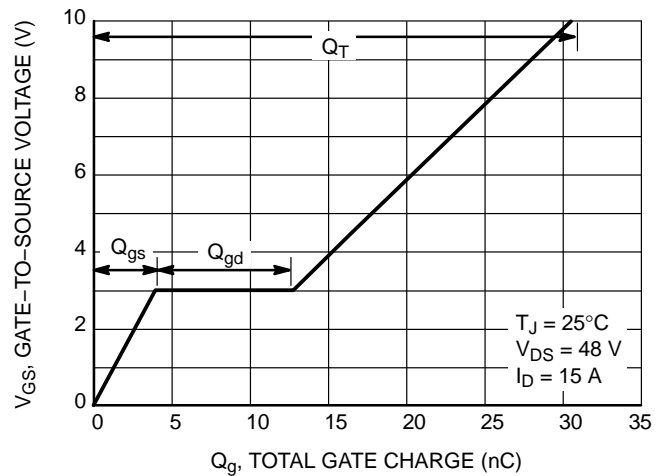


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

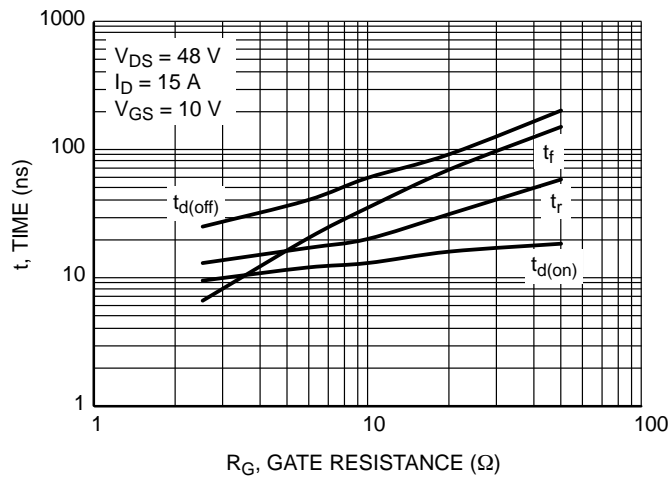


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

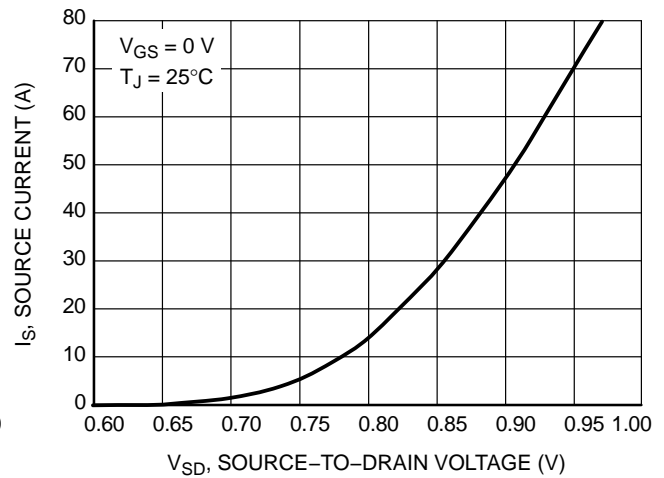


Figure 10. Diode Forward Voltage vs. Current

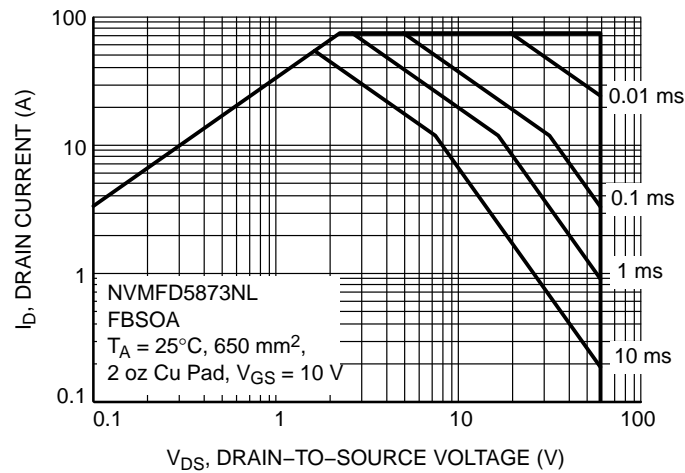


Figure 11. Maximum Rated Forward Biased Safe Operating Area

TYPICAL CHARACTERISTICS

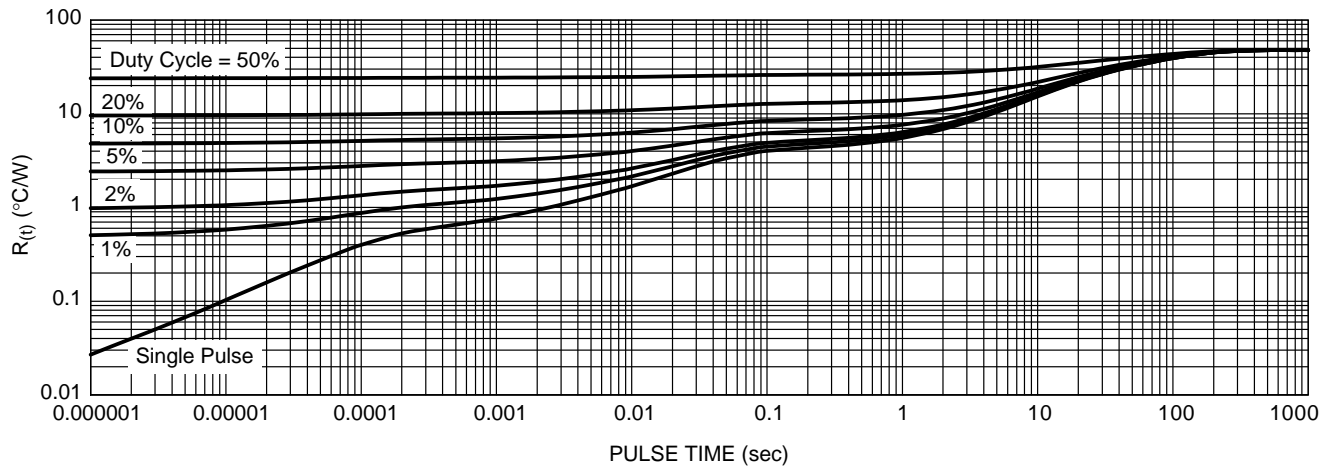
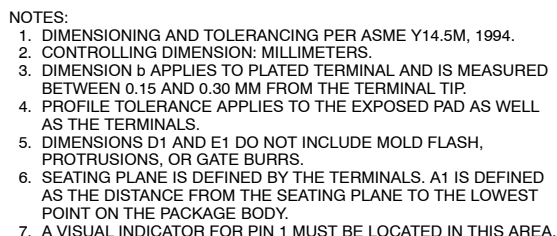


Figure 12. Thermal Response

**ON**



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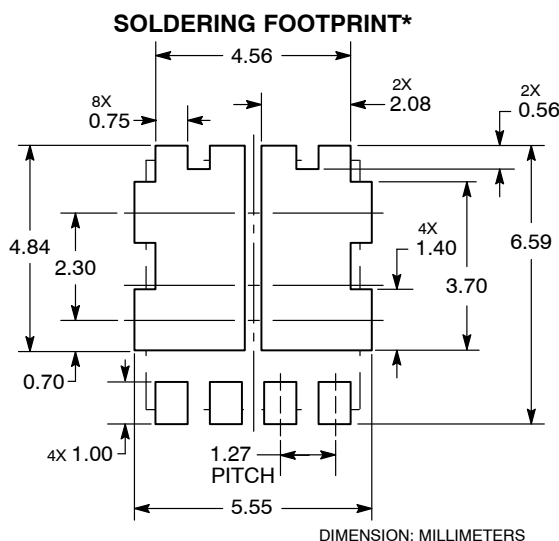


1 ○ XXXXXX  
AYWZZ

XXXXXX= Specific Device Code  
A = Assembly Location  
Y = Year  
W = Work Week  
ZZ = Lot Traceability

	MILLIMETERS		
DIM	MIN	MAX	MAX
A	0.90	-----	1.10
A1	-----	-----	0.05
b	0.33	0.42	0.51
b1	0.33	0.42	0.51
c	0.20	-----	0.33
D	5.15 BSC		
D1	4.70	4.90	5.10
D2	3.90	4.10	4.30
D3	1.50	1.70	1.90
E	6.15 BSC		
E1	5.70	5.90	6.10
E2	3.90	4.15	4.40
e	1.27 BSC		
G	0.45	0.55	0.65
h	-----	-----	12 °
K	0.51	-----	-----
K1	0.56	-----	-----
L	0.48	0.61	0.71
M	3.25	3.50	3.75
N	1.80	2.00	2.20


\*This information is generic. Please refer to device data sheet for actual part marking.



DIMENSION: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual. SOLDERRM/D.

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<b>DESCRIPTION:</b>	<b>DFN8 5X6, 1.27P DUAL FLAG (SO8FL-DUAL)</b>	<b>PAGE 1 OF 1</b>

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