S12ZVC/A/19/12/64/96 (HEARST)
ATMC VS TSMC10 CAPACITY EXPANSION

AUTOMOTIVE PROCESSORS
28-MAY-2021

180nm UHV Wafer Capacity Expansion

- Consistent with NXP's previous communications and in alignment with our policy of providing flexible sourcing and supply assurance, NXP qualified Carcassonne in Q4 2020 and has now completed qualification for Hearst (all 180nm UHV wafer technology) at Taiwan Semiconductor Manufacturing Company Fab 10 (TSMC10), Shanghai, China.

- NXP requires the use of Flex part numbers to maximize supply continuity and provide best possible lead time. Without the use of Flex part numbers, backlog will have to be converted from one fab sourced device to another fab sourced device as capacity dictates.
  - Carcassonne is the first MagniV product to be dual qualified, ATMC / TSMC10 in Q4 2020.
  - Knox128 and Tomar3 have successfully completed dual qualification, ATMC / TSMC10 in Q1 2021.
  - Knox32 have successfully completed dual qualification, ATMC / TSMC10 in Q2 2021.

TSMC10 Overview

- *High volume, 200mm fab F10-TSMC located in Shanghai, China*
  - *Fab Area: 24,000m*
  - *Low defectivity, high volume Accumulative 10M Wafer Out*
  - *Monthly capacity 130K wfr/month*
  - *follows the same quality system as tsmc cooperate HQ*
- *Production Status*
  - *>50 customers, >250 products, >1 million accumulated wafers*
- *Comprehensive Solution 0.5um~0.11um technology*
  - *3.3V or 5V I/O*
  - *High endurance or low leakage devices*
- *Automotive grade certified*
  - *Grade1 18HDR since 2014*
  - *ISO/IATF16949 since 2017*
  - *13 technology. Qualified on Grade 1; 23 products from 7 customers*
- *NXP-Fab10 business engagement*

Summary of Changes

Process Step	Changes	Details
Wafer Fab	• TSMC10 becomes a dual wafer source	• Process electrical characteristics matched • No Data Sheet specification changes
Design	• No Design changes	• No Design changes
Packaging	• Packages qualified with same Build of Material	• No difference in product performance
Marking	• Mask # is marked on product so that customers can visually distinguish ATMC or TSMC10.	• Slide #5 & #6 provides marking details
Test	• No Change to Test Flow, Specification or Quality	• No difference in product performance • Electrical Distributions (ED) comparison, ATMC vs TSMC, included in PCN
Reliability	• Passed AECQ100 qualification	• Qualification Report available within PCN
Orderable Part Numbers	• *Required conversion to "Flex" part number for supply assurance.*	• *Slide #5 & #6 provides part number details*

Changes within the AEC Q100 Certification of Design, Construction and Qualification (CofDC)

Supplier Name: NXP Semiconductors	Date: 10Jan2018	Date: 18March2021
Item Name	**Supplier Response**	**Supplier Response**
1. User's Part Number:	See PPAP	See PPAP
2. Supplier's Part Number/Data Sheet:	S9S12ZVC/A/19/12/64/96FxxLF/KH S9S12ZVC/A/19/12/64/96FxxLF/KH	S9S12ZVC/A/19/12/64/96AxxLF/KH S9S12ZVC/A/19/12/64/96AxxLF/KH
3. Device Description:	LL18UHV	LL18UHV
4. Wafer/Die Fab Facility & Process ID:		
a. Facility name/plant #:	NXP-ATMC	TSMC10
b. Street address:	3501 Ed Bluestein Boulevard; Austin, TX 78721 (ATMC)	4000, Wen Xiang Road, Songjiang, Shanghai, Postcode: 201616
c. Country:	USA	China
8. Wafer/Die:		
a. Wafer Size:	200mm	200mm
b. Die family:	SGF180	SGF180
c. Die mask set revision & name:	0N23N, 1N23N	0P81C, 1P81C
d. Die photo:	Available upon request	Available upon request
9. Die Technology Description:		
a. Wafer/Die process technology:	E018	E018
b. Die channel length (µM):	0.18	0.18
c. Die gate length (µM):	0.18	0.18
d. Die supplier process ID (mask #):	N23N	P81C
e. Number of transistors or gates:	Gates: 643609	Gates: 643609
f. Number of mask steps:	37	37
10. Die Dimensions:		
a. Die width (mm):	3.85	3.85
b. Die length (mm):	3.5	3.5
c. Die thickness (finished) (mm):	0.28	0.28
11. Die Metallization:		
a. Die metallization materials:	Al(0.5%Cu)	Al(0.5 wt%Cu)
b. Number of layers:	5	5
c. Thickness (per layer):	4KA (M1~M4), 8KA(LM)	M1~4: 4 kA, M5: 8kA
d. % of alloys (if present):	Al/Cu 0.5%	99.5% Al/0.5% Cu
12. Die Passivation:		
a. Number of passivation layers:	3	3
b. Die passivation material(s):	HDP Oxide+SRON+PEN	10kA HDP + 1.5kA PE-OX + 6kA PE-SN
c. Thickness (es) & tolerances:	10K HDP+1.5KSRON+6KPEN(+/-6.5%)	P1. HDPOX-10KA: target:10000A, SPEC +/-1000A P2. Oxide-1.5K: target:1500A, SPEC:+/-150A P3. SiN-6K: target: 6000A, SPEC: +/-700A

S12ZVC/A/19/12/64/96 (Hearst) Order Part Numbers and Marking

Required

ATMC PNs	TSMC10 PNs	Flex PNs	
S912ZVC/A ff F0 t pp / R	S912ZVC/A ff L0 t pp / R	S912ZVC/A ff A t pp / R	ff = Flash memory size 12 = 128Kb; 64 = 64Kb; 19 = 192Kb; 96 = 96Kb t = Temp range (W, M, V, C): min -40C to W = 150C, M = 125C, V = 105C, C = 85C pp = package; LF = 48LQFP; KH = 64LQFP-EP
F0 = ATMC 0 = Rev 0	L0 = TSMC10 0 = Rev 0	(No wafer fab designator) A = ATMC /TSMC10 Rev0	

Marking		ATMC	TSMC10	
Line 1	Logo			
Line 2	Base Part No.	S912ZVC/A ff t pp		
Line 3	Mask#	0N23N	0P81C	
Line 4	Trace code	ALYWZ		A =Assembly site L =Lot ID Y =Year; W=week Z =Sub lot

S12ZVC/A/19/12/64/96 (Hearst) Order Part Numbers and Marking

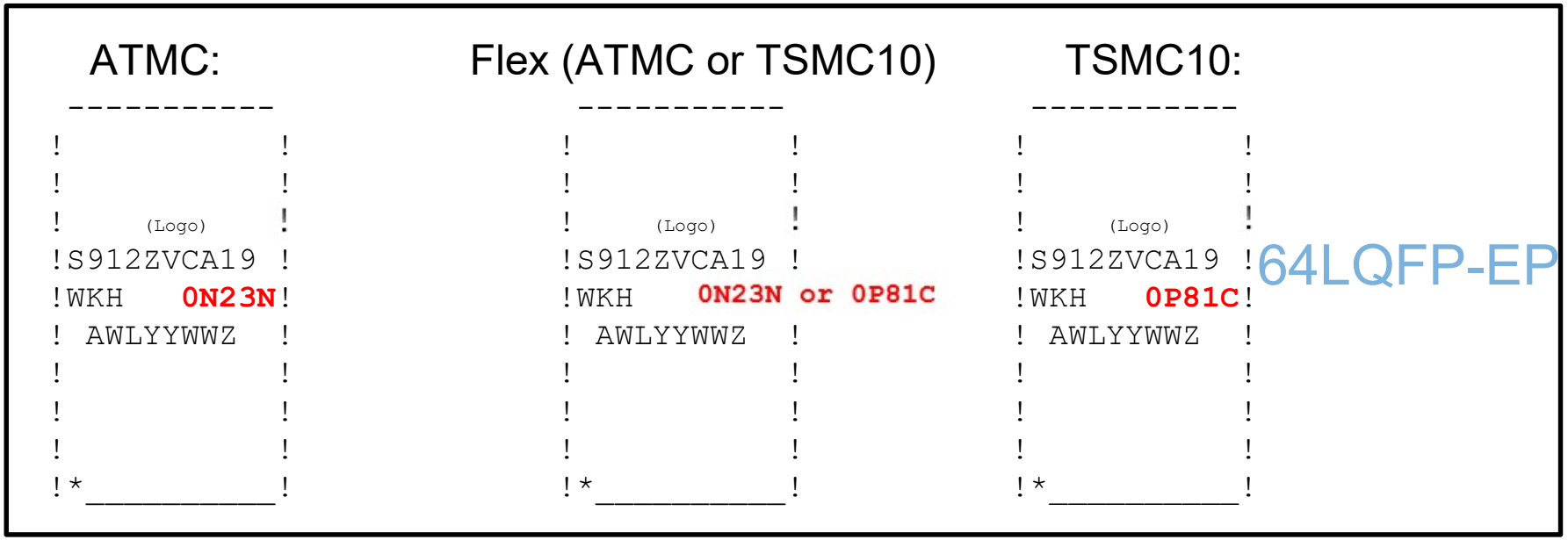
Required

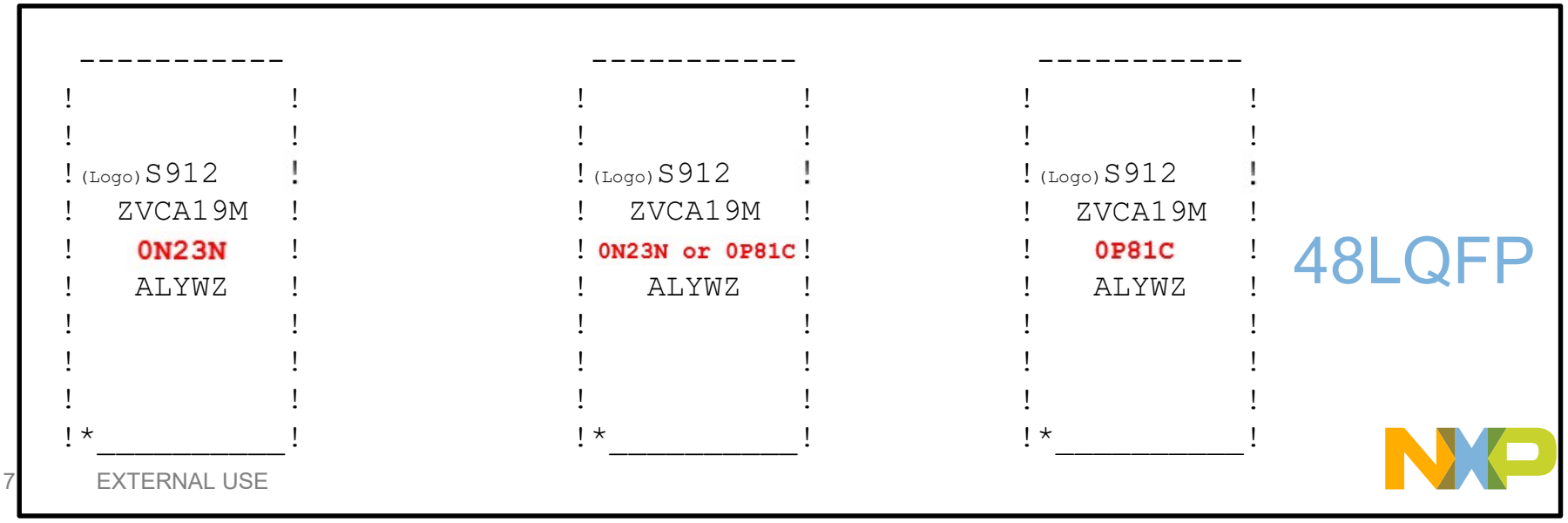
ATMC PNs	TSMC10 PNs	Flex PNs	
S912ZVC/A ff F1 t pp / R	S912ZVC/A ff L1 t pp / R	S912ZVC/A ff A1 t pp / R	ff = Flash memory size 12 = 128Kb; 64 = 64Kb; 19 = 192Kb; 96 = 96Kb t = Temp range (W, M, V, C): min -40C to W = 150C, M = 125C, V = 105C, C = 85C pp = package; LF = 48LQFP; KH = 64LQFP-EP
F1 = ATMC 1= Rev 1	L1 = TSMC10 1 = Rev 1	(No wafer fab designator) A1 = ATMC /TSMC10 Rev1	

Marking		ATMC	TSMC10	
Line 1	Logo			
Line 2	Base Part No.	S912ZVC/A ff t pp		
Line 3	Mask#	1N23N	1P81C	
Line 4	Trace code	ALYWZ		A =Assembly site L =Lot ID Y =Year; W=week Z =Sub lot

S12ZVC/A/19/12/64/96 (Hearst) Order Part Numbers and Marking

- ***How to distinguish between the ATMC and TSMC10 marking?***





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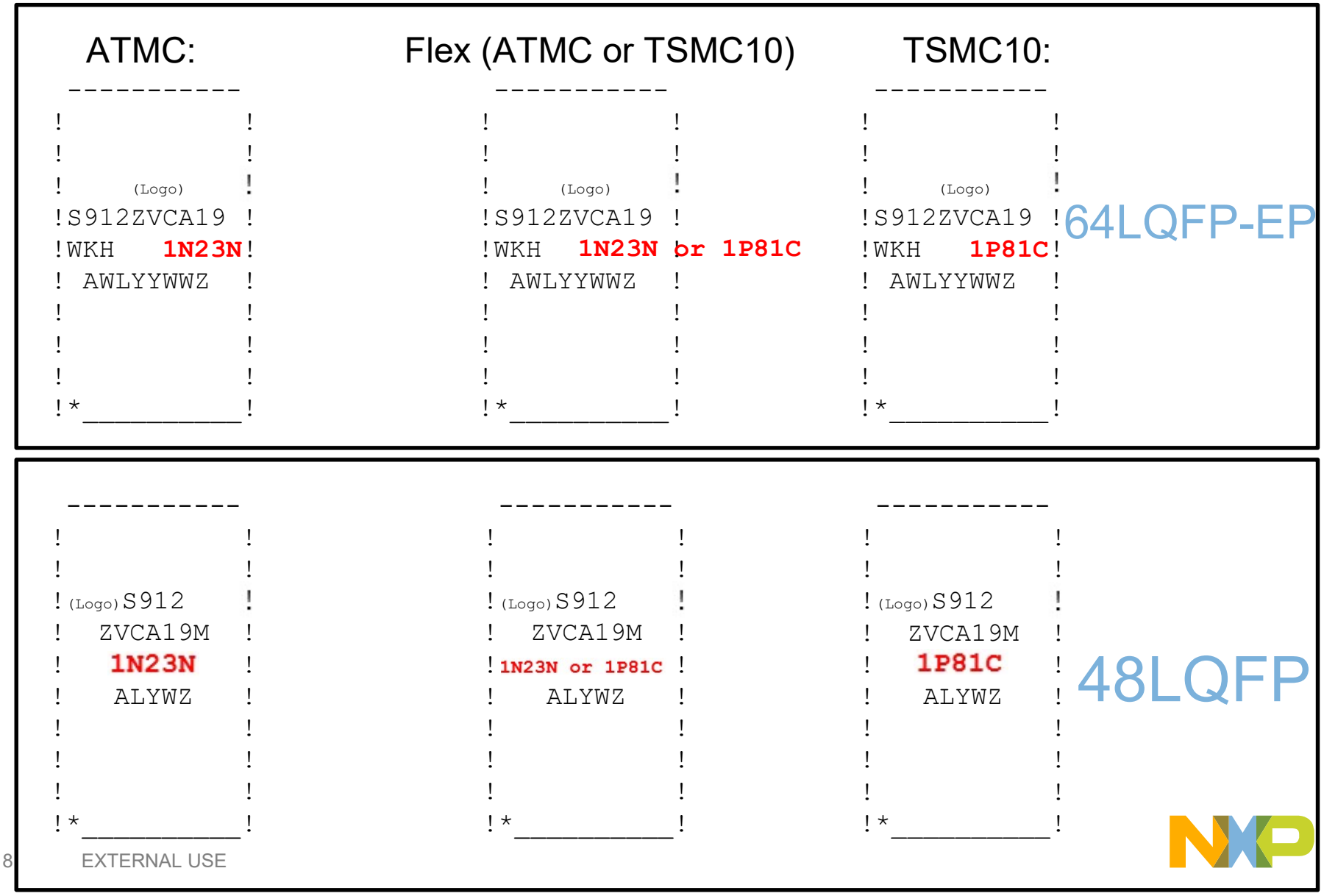

TSMC10 Part ID

Device	Mask Set Number	Part ID
MC9S12ZVCA64	0N23N	05.1D.10.00
	0P81C	
	1N23N	05.1D.10.01
	1P81C	
MC9S12ZVCA96	0N23N	05.1D.10.00
	0P81C	
	1N23N	05.1D.10.01
	1P81C	
MC9S12ZVCA128	0N23N	05.1D.10.00
	0P81C	
	1N23N	05.1D.10.01
	1P81C	
MC9S12ZVCA192	0N23N	05.1D.10.00
	0P81C	
	1N23N	05.1D.10.01
	1P81C	
MC9S12ZVC64	0N23N	05.1D.10.00
	0P81C	
	1N23N	05.1D.10.01
	1P81C	
MC9S12ZVC96	0N23N	05.1D.10.00
	0P81C	
	1N23N	05.1D.10.01
	1P81C	
MC9S12ZVC128	0N23N	05.1D.10.00
	0P81C	
	1N23N	05.1D.10.01
	1P81C	
MC9S12ZVC192	0N23N	05.1D.10.00
	0P81C	
	1N23N	05.1D.10.01
	1P81C	

TSMC10 mask set Part ID used the same with ATMC N23N.

No other register difference between two Fabs.

TSMC10 mask set P81C will be included in the updated Data Sheet.

S12ZVC/A/19/12/64/96 (Hearst) TSMC10 Expansion - Table below provides sample part numbers:

ATMC Part #	TSMC10 Qualified Sample Part #	Package
S912ZVC19F0MLF	K912ZVC19L0MLF	48LQFP
S912ZVC19F0VLF	K912ZVC19L0VLF	48LQFP
S912ZVC19F0VLFR	K912ZVC19L0VLFR	48LQFP
S912ZVC64F0VLFR	K912ZVC64L0VLFR	48LQFP
S912ZVC96F0MLFR	K912ZVC96L0MLFR	48LQFP
S912ZVC19F1WLFR	K912ZVC19L1WLFR	48LQFP
S912ZVCA19F1WLFR	K912ZVCA19L1WLFR	48LQFP

For custom part number samples, please check with your NXP representative for availability.

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