

Product / Process Change Notice

PCN No.: Q000-PCN-WF202305-02A

Date: 2023-11-22.

<p>Change Title: <u>Add SMIC as new fabrication site for NAU88C22YG & NAU88C22IG products.</u></p> <p>Change Classification: <input checked="" type="checkbox"/> Major <input type="checkbox"/> Minor</p> <p>Change item: <input type="checkbox"/> Design <input type="checkbox"/> Raw Material <input checked="" type="checkbox"/> Wafer FAB <input type="checkbox"/> Package Assembly <input type="checkbox"/> Testing <input type="checkbox"/> Others: _____.</p>
<p>Affected Product(s) :</p> <p>The affected parts are NAU88C22YG and NAU88C22IG.</p>
<p>Description of Change(s) :</p> <p>Add new fabrication site for affected parts at SMIC (Semiconductor Manufacturing International Corporation) as the 2nd source.</p> <p><u>New Supplier</u></p> <p>Semiconductor Manufacturing International Corporation (hereinafter “SMIC”), (No.18 Gaoxin Road, Export Processing Zone, Pingshan New Area, Shenzhen 518118 People’s Republic of China)</p>
<p>Reason for Change(s) :</p> <p>To increase manufacturing capacity, flexibility and enhance disaster recovery</p>
<p>Impact of Change(s) : (positive & negative)</p> <p>Form: The topside mark of the affected parts will have a letter which is different in red color. The following picture indicate the anticipated product topside mark change. The letter “B” in the position marked in red will be different to the original letter” A”.</p> <div style="display: flex; justify-content: space-around; align-items: center;"> <div style="border: 1px solid black; padding: 5px; text-align: center;"> <p>NAU88C22</p> <p>YG 914</p> <p>AA 123456</p> <p>● 78-11</p> </div> <div style="border: 1px solid black; padding: 5px; text-align: center;"> <p>NAU88C22</p> <p>IG 914</p> <p>AA 123456</p> <p>● 78-11</p> </div> </div> <p>Fit: No change.</p> <p>Function: No change.</p> <p>Reliability: No concern (passed the qualification)</p> <p>HSF (Hazardous Substances Free): No change</p>
<p>Qualification Plan/ Results :</p> <p>Passed the Nuvoton’s reliability qualification includes ESD, LU, HTOL, Pre-conditioning, THB, TCT, uHAST and HTSL, please refer to appendix A for details.</p>

Implementation Plan :

1. Samples for customer evaluation are available and can be provided immediately.
2. Approval is necessary as early as possible to start manufacturing.

Date Code: _____ onward Lot No.: _____ onward Implemented date: Feb. 20, 2024

Originator:	H.Y. Lai / Q100	Approval:(QRA Director)	C.H. Shen/ Q000
Contact for Questions & Concerns	Name: <u>HYLai</u> TEL: <u>886-3-5770066 (ext. 31226)</u> FAX: <u>886-3-5792673</u> . Address: <u>No.4, Creation Rd. III Science-Based Industrial Park Hsinchu, Taiwan, R.O.C.</u> E-mail: <u>hylai0@nuvoton.com</u> .		

Customer Comments:

Note: Please sign this notice, and return to **Nuvoton** contact within **30** days. If no response is received within **30** days, this Change Request will be assumed to meet your approval.

<input type="checkbox"/> Approval <input type="checkbox"/> Disapproval <input type="checkbox"/> Conditional Approval: _____
Date: _____ Dept. name: _____ Person in charge: _____

Follow-up and Tracing:

A. copies to

FAB: Integration _____ _____ _____ _____ _____

Test / Product: UL40 Long Chieu UL40 Simon Wilson AS60 CHTsai AS70 JWCheng.

Design/ Marketing: UL00 Mark Hemming AM00 CPLin AM20 KPTsai.

Production control/ Others: P100 YLHsu P100 CHHsu FD20 SPTsai FD20 CCChen.

B. Changes:

1. Document / Test program:

Document No/ test program	Document name/ test program name	Version		Responsible	Completed date	Remark
		before	after			
NA	NA	NA	NA	NA	NA	NA

Verified by: _____

Appendix A: Nuvoton qualification report

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RELIABILITY REPORT

NAU88C22YGC

FUNCTION : Stereo Audio CODEC

PROCESS : SMIC 0.153um

ENGINEER : *HYLi*

MANAGER : *JTLiu*

Publication Release Date: Jun. 2023

Reliability Engineering Department

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~SUMMARY~

NAU88C22YGC with QFN32 passed the qualification tests according to Nuvoton product qualification requirement. A summary of the test result is as follows:

℞. High Temperature Operating Life	: 0/231 pcs
℞. High Temperature Storage Life	: 0/231 pcs
℞. Preconditioning	: 0/693 pcs
℞. Temperature Humidity Bias	: 0/231 pcs
℞. Unbiased Highly Accelerated Stress Test	: 0/231 pcs
℞. Temperature Cycling	: 0/231 pcs
℞. ESD-HBM	: 0/48 pcs
℞. ESD-CDM	: 0/6 pcs
℞. Latch-Up	: 0/6 pcs

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1. Preconditioning (PC)
2. Temperature Humidity Bias (THB)
3. Unbiased Highly Accelerated Stress Test (UHAST)
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B. Test Results

1. Preconditioning (PC)
2. Temperature Humidity Bias (THB)
3. Unbiased Highly Accelerated Stress Test (UHAST)
4. Temperature Cycling (TC)

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IV. ESD AND LATCH-UP

A. Introduction

1. ESD
2. Latch-Up

B. Test Results

1. ESD
2. Latch-Up

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I. PRODUCT DESCRIPTION

General Description

The NAU88C22YGC is a low power, high quality CODEC for portable and general purpose audio applications. In addition to precision 24-bit stereo ADCs and DACs, this device integrates a broad range of additional functions to simplify implementation of complete audio system solutions. The NAU88C22YGC includes drivers for speaker, headphone, and differential or stereo line outputs, and integrates preamps for stereo differential microphones, significantly reducing external component requirements. Also, a fractional PLL is available to accurately generate any audio sample rate for the CODEC using any commonly available system clock from 8MHz through 33MHz.

Advanced on-chip digital signal processing includes a 5-band equalizer, a 3-D audio enhancer, a mixed-signal automatic level control for the microphone or line input through the ADC, and a digital limiter/dynamic-range-compressor (DRC) function for the playback path. Additional digital filtering options are available in the ADC path, to simplify implementation of specific application requirements such as "wind noise reduction" and speech band enhancement. The digital audio input/output interface can operate as either a master or a slave.

The NAU88C22YGC operates with analog supply voltages from 2.5V to 3.6V, while the digital core can operate at 1.7V to conserve power. The loudspeaker BTL output pair and two auxiliary line outputs can operate using a 5V supply to increase output power capability, enabling the NAU88C22YGC to drive 1 Watt into an external speaker. Internal register controls enable flexible power saving modes by powering down sub-sections of the chip under software control.

The NAU88C22YGC is specified for operation from -40°C to +85°C, and is available in a space-saving 32-lead QFN package.

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II. LIFE TEST

A. Introduction

1. High Temperature Operating Life (HTOL)

1.1 SCOPE

HTOL test is to accelerate failure mechanisms which are thermally activated. This can be achieved by stressing the device with bias at high temperature.

1.2 TEST CONDITION

T_A (Temperature Ambient) = 125°C, VDD1 = 3.6V, VDD2 = 5.5V, dynamic stressing, T_d = 168, 500, 1000 hrs.
(Reference: JESD22-A108)

2. High Temperature Storage Life (HTSL)

2.1 SCOPE

HTSL test is to determine the stability of device in high temperature environment.

2.2 TEST CONDITION

T_A (Temperature Ambient) = 150°C, T_d = 168, 500, 1000 hrs.
(Reference: JESD22-A103)

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B. Test Results

1. High Temperature Operating Life (HTOL)

1.1 SUMMARY TABLE

Run	Lot No.	168 hrs	500 hrs	1000 hrs	Remark
#1	E204E008-ZY	0/77	0/77	0/77	PASS
#2	E240E005-ZY	0/77	0/77	0/77	PASS
#3	E241E004-ZY	0/77	0/77	0/77	PASS

*Criteria: Acc/Rej = 0/1

1.2 FAILURE RATE CALCULATION

$$F.R.(T) = \frac{\chi^2 (1 - CL, 2N + 2)}{2 EDH}$$

WHERE χ^2 : CHI-SQUARE Function

CL: Confidence Level

N: No of Failures

EDH: Equivalent Device Hour

Dev. Hours at Tj= 126.2°C	Equiv. Dev. Hours at Tj=55°C	No. of Failure	Confidence Level	Failure Rate at 55°C	Mean Time Between Failure
231000	19143614.9	0	60%	47.8 FIT	2384 yrs.
			90%	120.2 FIT	949 yrs.

Activation Energy = 0.7 eV

$T_j = T_a + P_d \cdot \theta_{ja}$ where: Tj= junction temp, Ta=125°C(ambient temp)

Pd= 37.6mW (power dissipated on the device)

θ_{ja} = 32.3°C/W (thermal resistance from junction to ambient)

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2. High Temperature Storage Life (HTSL)

Run	Lot No.	168 hrs	500 hrs	1000 hrs	Remark
#1	E204E008-ZY	0/77	0/77	0/77	PASS
#2	E240E005-ZY	0/77	0/77	0/77	PASS
#3	E241E004-ZY	0/77	0/77	0/77	PASS

*Criteria: Acc/Rej = 0/1

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III. ENVIRONMENTAL TEST

A. Introduction

1. Preconditioning (PC)

1.1 SCOPE

PC test is to measure the resistance of SMD (Surface Mount Devices) to the storage environment at the customer site and to thermal stress created by IR reflow or Vapor Phase Reflow.

1.2 TEST CONDITION

Step 1: TC (-65°C/150°C, 5 cycles)
Step 2: Bake (125°C, 24 hours)
Step 3: Soak (30°C/60%RH, 192 hours)
Step 4: IR 260°C, 3 passes
(Reference: JESD22-A113)

2. Temperature Humidity Bias (THB)

2.1 SCOPE

THB test is to measure the moisture resistance of plastic encapsulated circuit.

2.2 TEST CONDITION

T_A (Temperature Ambient) = 85°C, Humidity = 85%RH, VDD1 = 3.6V,
VDD2 = 5.5V, Alternating Pin Bias, T_d = 168, 500, 1000 hrs.
(Reference: JESD22-A101)

3. Unbiased Highly Accelerated Stress Test (UHAST)

3.1 SCOPE

UHAST test is to evaluate the device resistance to moisture penetration.

3.2 TEST CONDITION

T_A (Temperature Ambient) = 130°C, RH = 85%, T_d = 96 hrs.
(Reference: JESD22-A118)

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4. Temperature Cycling (TC)

4.1 SCOPE

TC test is to evaluate the resistance of device to environmental temperature change.

4.2 TEST CONDITION

-65°C / +150°C, 500 cycles.
(Reference: JESD22-A104)

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B. Test Results

1. Preconditioning (PC)

Run	Lot No.	Result	Remark
#1	E204E008-ZY	0/154	PASS
#2	E240E005-ZY	0/154	PASS
#3	E241E004-ZY	0/154	PASS
#4	E240E005-ZX	0/77	PASS
#5	E240E005-ZV	0/77	PASS
#6	E240E005-ZT	0/77	PASS

*Criteria: Acc/Rej = 0/1

2. Temperature Humidity Bias (THB)

Run	Lot No.	168 hrs	500 hrs	1000 hrs	Remark
#1	E204E008-ZY	0/77	0/77	0/77	PASS
#2	E240E005-ZY	0/77	0/77	0/77	PASS
#3	E241E004-ZY	0/77	0/77	0/77	PASS

*Criteria: Acc/Rej = 0/1

3. Unbiased Highly Accelerated Stress Test (UHAST)

Run	Lot No.	96 hrs	Remark
#1	E204E008-ZY	0/77	PASS
#2	E240E005-ZY	0/77	PASS
#3	E241E004-ZY	0/77	PASS

*Criteria: Acc/Rej = 0/1.

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4. Temperature Cycling (TC)

Run	Lot No.	500 cycles	Remark
#1	E240E005-ZX	0/77	PASS
#2	E240E005-ZV	0/77	PASS
#3	E240E005-ZT	0/77	PASS

*Criteria: Acc/Rej = 0/1.

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IV. ESD AND LATCH-UP

A. Introduction

1. ESD

1.1 SCOPE

ESD test is to evaluate the immunity of device to electrostatic discharge.

1.2 TEST CONDITION

Human Body Model (HBM): JS-001

Charged Device Model (CDM): JS-002

2. Latch-Up

2.1 SCOPE

Latch-Up test is to evaluate the immunity of device to latch-up.

2.2 TEST CONDITION

JEDEC STD-78F.01, T_A (Temperature Ambient) = 25°C, Vddmax
Operating Voltage.

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B. Test Results

1. ESD

1.1 Human Body Model

Run	Lot No.	Positive	Negative	Remark
#1	E204E008-ZY	0/24	0/24	PASS

*Criteria: Acc/Rej = 0/1.

*| stress level | = 2KV

1.2 Charged Device Model

Run	Lot No.	Positive	Negative	Remark
#1	E204E008-ZY	0/3	0/3	PASS

*Criteria: Acc/Rej = 0/1.

*| stress level | = 500V

2. Latch-Up

Run	Lot No.	Positive	Negative	Remark
#1	E204E008-ZY	0/3	0/3	PASS (Class I.A)

*Criteria: Acc/Rej = 0/1.

*| stress level | = 100mA, Overvoltage = 5.4V & 8.25V

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