400G-DR4 OSFP Transceiver

FEATURES:

- Hot-pluggable OSFP 400G DR4 single mode transceiver
- Compliant with OSFP-RHS
- Compliant with CMIS 4.0
- Maximum power consumption 9W
- Compliant with IEEE 802.3-2022: 400GBASE-DR4 optical interface
- Compliant with IEEE 802.3ck-2022: 400GAUI-4/200GAUI-2/100GAUI-1 C2M electrical interface
- IB NDR support
- Case operating temperature 0°C to 70°C
- Two wire serial Interface with digital diagnostic monitoring
- Complies with EU Directive 2011/65/EU (RoHS compliant)
- Class 1 Laser

I. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Storage Temperature	T_S	-40	85	ºC	
Supply Voltage	V_{CC}	-0.5	3.6	V	
Relative Humidity (non-condensing)	RH	5	95	%	
Control Input Voltage	V_I	-0.3	V_{CC}+0.5	V	

II. Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	T_{OPR}	0	-	70	ºC	
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Instantaneous peak current at hot plug	I_{CC_IP}	-	-	3600	mA	
Sustained peak current at hot plug	I_{CC_SP}	-	-	2997	mA	
Maximum Power Dissipation	P_D	-	-	9	W	
Maximum Power Dissipation, Low Power Mode	P_{DLP}	-	-	2	W	
Signaling Rate per Lane	SRL	-	53.125	-	GBd	
Two Wire Serial Interface Clock Rate	-	-	-	400	kHz	

Power Supply Noise Tolerance 1 kHz – 1 MHz (p-p)	-	-	-	66	mVpp	
Operating Distance	-	2	-	500	m	

III. Transmitter Optical Specifications

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Wavelength	λ_C	1304.5	1311	1317.5	nm	
Side Mode Suppression Ratio	SMSR	30	-	-	dB	
Average Launch Power, each lane	AOP_L	-2.9	-	4.0	dBm	1
Outer Optical Modulation Amplitude (OMA_{outer}), each lane	T_{OMA}	-0.8		4.2	dBm	
Launch power in OMA_{outer} minus TDECQ, each lane	$T_{OMA-TDECQ}$	-2.2	-	-	dBm	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each lane	TDECQ	-	-	3.4	dB	
Average Launch Power of OFF Transmitter, each lane	T_{OFF}	-	-	-15	dBm	
Extinction Ratio, each lane	ER	3.5		-	dB	
$RIN_{21.4}OMA$	RIN	-	-	-136	dB/Hz	
Optical Return Loss Tolerance	ORL	-	-	21.4	dB	
Transmitter Reflectance	T_R	-	-	-26	dB	2

Notes

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength.
2. Transmitter reflectance is defined looking into the transmitter.

IV. Receiver Optical Specifications

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Wavelength	λ_C	1304.5	1311	1317.5	nm	
Damage Threshold, average optical power, each lane	AOP_D	5	-	-	dBm	
Average Receive Power, each lane	AOP_R	-5.9	-	4.0	dBm	
Receive Power (OMA_{outer}), each lane	OMA_R	-	-	4.2	dBm	
Receiver Reflectance	RR	-	-	-26	dB	
Receiver Sensitivity (OMA_{outer}), each lane	S_{OMA}	-	-	Max(-3.9,SECQ-5.3	dBm	1
Stressed Receiver Sensitivity (OMA_{outer}), each lane	SRS	-	-	-1.9	dBm	2
Conditions of stressed receiver sensitivity test						
Stressed eye closure for PAM4	SECQ	-	3.4	-	dB	
OMA_{outer} of each aggressor lane	-	-	4.2	-	dBm	

Notes:

1. Receiver sensitivity (OMA_{outer}), each lane (max) is informative and is defined for a transmitter with a value of SECQ up to 3.4 dB.
2. Measured with conformance test signal at TP3 for the BER = $2.4x10^{-4}$

V. Electrical Specification High Speed Signal

Receiver (Module Output, TP4)

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Differential output Voltage (Long mode)		-	-	845	mV	
Differential output Voltage (Short mode)		-	-	600	mV	
Eye height	EH	15	-	-	mV	
Vertical eye closure	VEC	-	-	12	dB	
Common-mode to differential-mode return loss	RLDc	802.3ck 120G-1			dB	
Effective return loss	ERL	8.5	-	-	dB	
Differential Termination Mismatch		-	-	10	%	
Transition Time (min, 20% to 80%)		8.5	-	-	ps	
DC common mode Voltage		-350	-	2850	mV	

Transmitter (Module Input, TP1)

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Differential pk-pk input Voltage tolerance (TP1a)	-	750	-	-	mV	
Differential-mode to common-mode return loss	RLcd	802.3ck 120G-2			dB	
Effective return loss	ERL	8.5	-	-	dB	
Differential termination mismatch	-	-	-	10	%	
Single-ended voltage tolerance range	-	-0.4	-	3.3	V	
DC common-mode voltage tolerance	-	-0.35	-	2.85	V	

VI. Electrical Specification Low Speed Signal

Parameter	Symbol	Min.	Max.	Unit	Notes
Module output SCL and SDA	V_{OL}	0	0.4	V	
	V_{OH}	V_{CC}-0.5	V_{CC}+0.3	V	
Module Input SCL and SDA	V_{IL}	-0.3	V_{CC}*0.3	V	
	V_{IH}	V_{CC}*0.7	V_{CC}+0.5	V	
InitMode, ResetL and ModSelL	V_{IL}	-0.3	0.8	V	
	V_{IH}	2	V_{CC}+0.3	V	
IntL	V_{OL}	0	0.4	V	
	V_{OH}	$V_{CC-0.5}$	V_{CC}+0.3	V	

VII. Pin Definitions

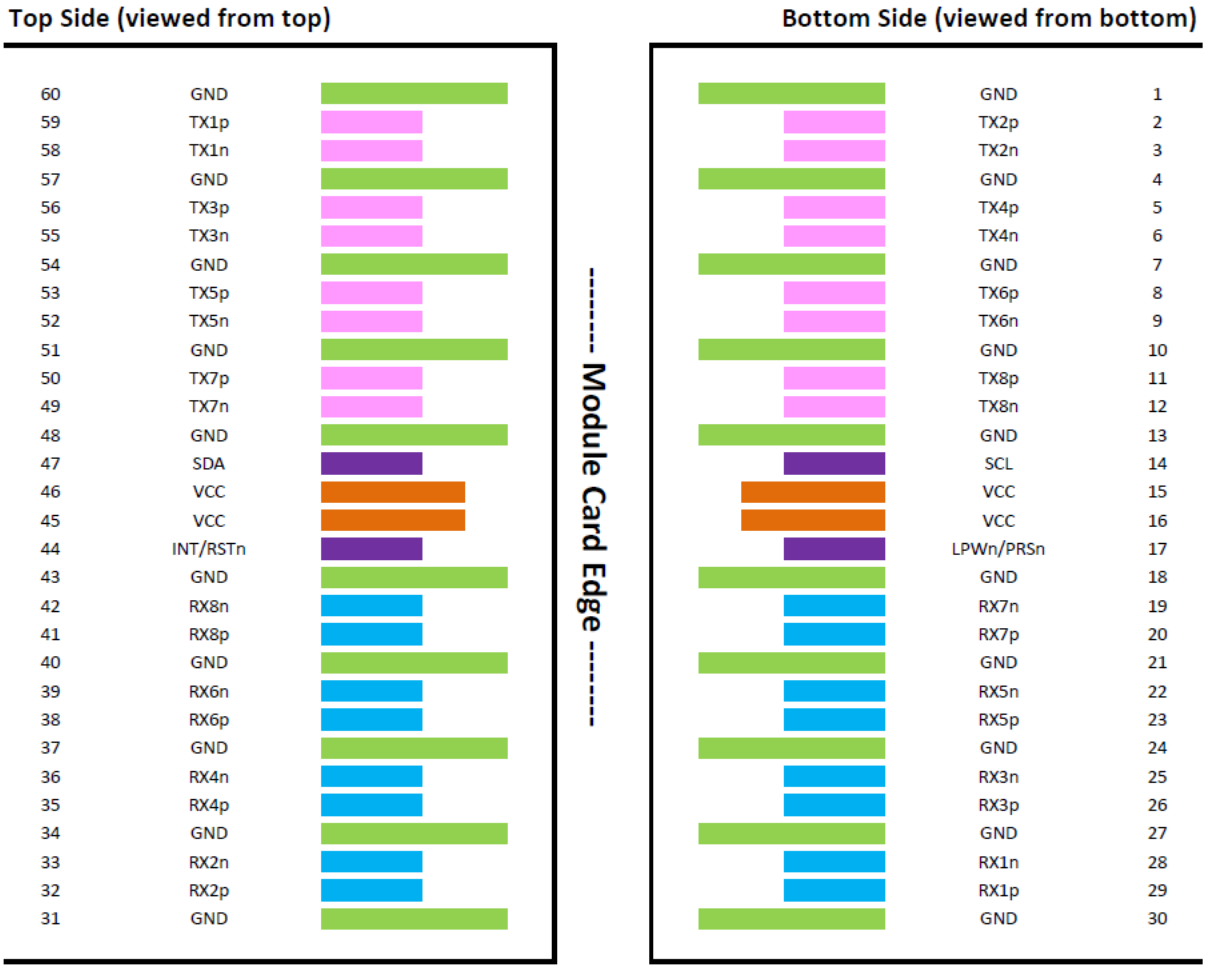

Figure 1 – OSFP module Pinout

Pin#	Logic	Symbol	Description	Direction	Plug Sequence	Notes
1		GND	Ground		1	
2	CML-I	TX2p	Transmitter Data Non-Inverted	Input from Host	3	
3	CML-I	TX2n	Transmitter Data Inverted	Input from Host	3	
4		GND	Ground		1	
5	CML-I	TX4p	Transmitter Data Non-Inverted	Input from Host	3	
6	CML-I	TX4n	Transmitter Data Inverted	Input from Host	3	
7		GND	Ground		1	
8	CML-I	TX6p	Transmitter Data Non-Inverted	Input from Host	3	Not used
9	CML-I	TX6n	Transmitter Data Inverted	Input from Host	3	Not used
10		GND	Ground		1	
11	CML-I	TX8p	Transmitter Data Non-Inverted	Input from Host	3	Not used

12	CML-I	TX8n	Transmitter Data Inverted	Input from Host	3	Not used
13		GND	Ground		1	
14	LVCMOS-I/O	SCL	2-wire Serial interface clock	Bi-directional	3	
15		VCC	+3.3V Power	Power from Host	2	
16		VCC	+3.3V Power	Power from Host	2	
17	Multi-Level	LPWn/PRSn	Low-Power Mode / Module Present	Bi-directional	3	
18		GND	Ground		1	
19	CML-O	RX7n	Receiver Data Inverted	Output to Host	3	Not used
20	CML-O	RX7p	Receiver Data Non-Inverted	Output to Host	3	Not used
21		GND	Ground		1	
22	CML-O	RX5n	Receiver Data Inverted	Output to Host	3	Not used
23	CML-O	RX5p	Receiver Data Non-Inverted	Output to Host	3	Not used
24		GND	Ground		1	
25	CML-O	RX3n	Receiver Data Inverted	Output to Host	3	
26	CML-O	RX3p	Receiver Data Non-Inverted	Output to Host	3	
27		GND	Ground		1	
28	CML-O	RX1n	Receiver Data Inverted	Output to Host	3	
29	CML-O	RX1p	Receiver Data Non-Inverted	Output to Host	3	
30		GND	Ground		1	
31		GND	Ground		1	
32	CML-O	RX2p	Receiver Data Non-Inverted	Output to Host	3	
33	CML-O	RX2n	Receiver Data Inverted	Output to Host	3	
34		GND	Ground		1	
35	CML-O	RX4p	Receiver Data Non-Inverted	Output to Host	3	
36	CML-O	RX4n	Receiver Data Inverted	Output to Host	3	
37		GND	Ground		1	
38	CML-O	RX6p	Receiver Data Non-Inverted	Output to Host	3	Not used
39	CML-O	RX6n	Receiver Data Inverted	Output to Host	3	Not used
40		GND	Ground		1	
41	CML-O	RX8p	Receiver Data Non-Inverted	Output to Host	3	Not used
42	CML-O	RX8n	Receiver Data Inverted	Output to Host	3	Not used
43		GND	Ground		1	
44	Multi-Level	INT/RSTn	Module Interrupt / Module Reset	Bi-directional	3	
45		VCC	+3.3V Power	Power from Host	2	
46		VCC	+3.3V Power	Power from Host	2	
47	LVCMOS-I/O	SDA	2-wire Serial interface data	Bi-directional	3	
48		GND	Ground		1	
49	CML-I	TX7n	Transmitter Data Inverted	Input from Host	3	Not used
50	CML-I	TX7p	Transmitter Data Non-Inverted	Input from Host	3	Not used
51		GND	Ground		1	
52	CML-I	TX5n	Transmitter Data Inverted	Input from Host	3	Not used
53	CML-I	TX5p	Transmitter Data Non-Inverted	Input from Host	3	Not used
54		GND	Ground		1	
55	CML-I	TX3n	Transmitter Data Inverted	Input from Host	3	
56	CML-I	TX3p	Transmitter Data Non-Inverted	Input from Host	3	
57		GND	Ground		1	
58	CML-I	TX1n	Transmitter Data Inverted	Input from Host	3	
59	CML-I	TX1p	Transmitter Data Non-Inverted	Input from Host	3	
60		GND	Ground		1	

VIII. Recommended OSFP Host Board Schematic

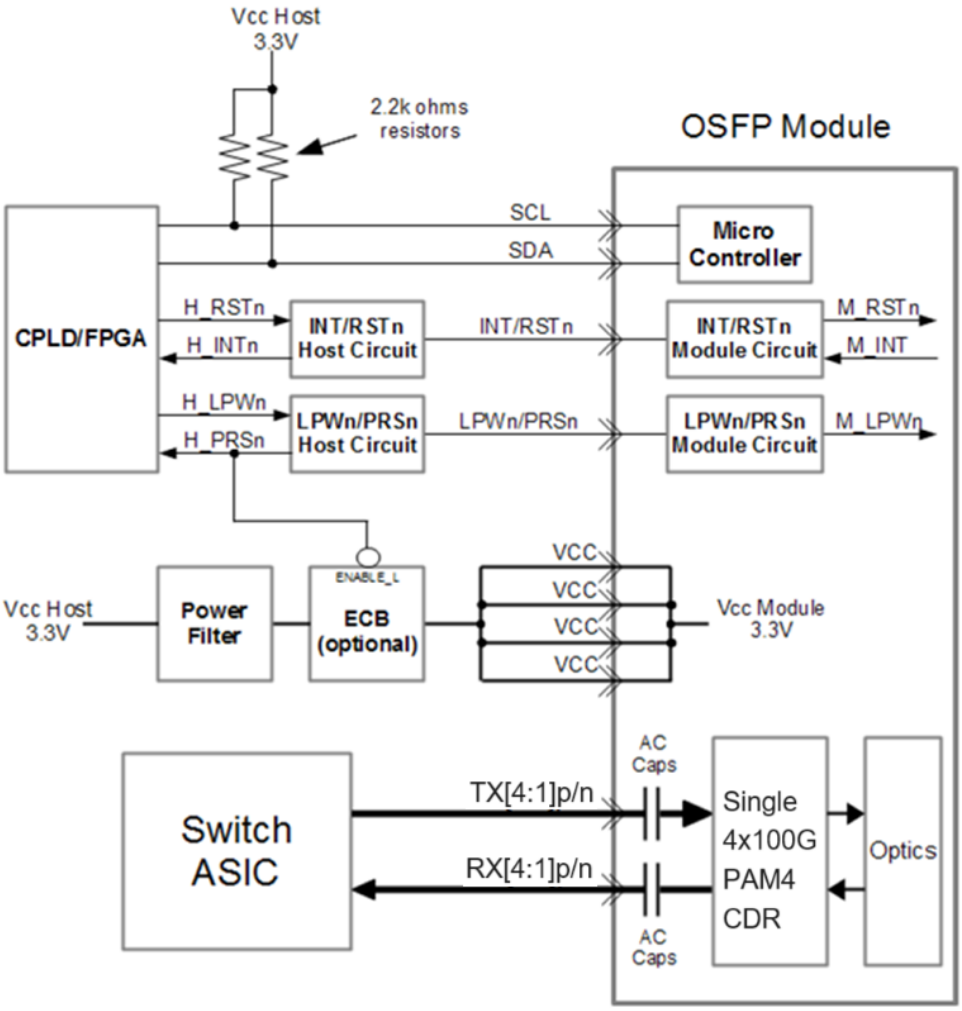

Figure 2 – Recommended OSFP Host Board Schematic

IX. Mechanical Dimensions

TBD

X. Ordering Information

Part Number	Description
O-100N-OR-DR4	Single-port, 400Gb/s, OSFP, MPO, 1,310nm SMF, DR4, up to 150m, Flat top RHS